APPARATUS AND METHOD FOR COMPENSATING A HIGH IMPEDANCE ATTENUATOR

Field of the Invention

The subject invention generally concerns the field of circuitry for compensating attenuators to correct for errors caused by stray capacitance, and specifically concerns novel architecture for such compensating circuitry.

Background of the Invention

High impedance attenuators are commonly used in modern digital test equipment, such as oscilloscopes, digital multimeters, and the like, to greatly reduce undesirable interaction with (i.e., loading of) a circuit under test. Attenuators also serve to reduce large amplitude signals to prevent overloading of the input signal amplifier (i.e., front end) of the test and measurement instrument.

Typical high impedance attenuators for use with oscilloscopes exhibit a 10:1 attenuation of the input signal. Such attenuators normally employ a resistor-capacitor (R-C) voltage dividing arrangement and an amplifier. In such arrangements variation in the resistances is not a problem because highly accurate resistors are generally available. That is highly accurate DC attenuators are easily realized. However, variation in the capacitance values of the capacitors is much more of a problem. For this reason, those skilled in the attenuator art have traditionally chosen to adjust the capacitors, rather than adjust the resistors. High impedance attenuators are vulnerable to the effects of stray capacitance variation because the capacitors they use are small in value. Variations in circuit board traces of the attenuator, variations in the values of its components, and variations in its own input amplifier, all contribute to changes in high frequency attenuation. Unfortunately, these variations and variation in input capacitance values and stray capacitance adversely affect the operation of these attenuators by distorting the leading edges of signals under test.

Prior art attempts at correcting this problem have met with some success but have generally introduced problems of their own. For example, hand adjustment of variable capacitors is an unreliable procedure. One solution to this problem is to use electronically

variable capacitors (varactor diodes), but unfortunately, varactor diodes are inherently non-linear. Other problems may further include the introduction of noise by variable gain amplifiers driving capacitive feedback, frequency-dependent problems, such as phase delay, or problems related to requiring a variable gain amplifier to absorb a significant portion of a high-frequency input current.

What is needed is a relatively inexpensive compensated attenuator circuit, for use in a test and measurement instrument, which does not exhibit, or which reduces the effects of, the undesirable traits listed above.

Summary of the Invention

A high impedance attenuator for use in a test and measurement instrument employs compensation to adjust the low frequency attenuation to match the high frequency attenuation exhibited by the attenuator, rather than attempting to adjust the high frequency attenuation exhibited by the attenuator.

In an alternate embodiment of the invention, compensation to adjust low frequency attenuation is employed in a feedback loop and an opposite resistance is applied in an additional attenuator stage to stabilize the input resistance.

In yet another embodiment of the invention, compensation to adjust low frequency attenuation is employed by means of an R-C time constant of an additional R-C circuit in a feed forward loop. This additional time constant is matched to the R-C time constant of the input R-C network. The input resistance of the attenuator is not changed.

Brief Description of the Drawing

FIGURE 1 shows an attenuator circuit having adjustable compensation, as known from the prior art.

FIGURE 2 shows another attenuator circuit having adjustable compensation, as known from the prior art.

FIGURE 3 shows an attenuator circuit having adjustable compensation in accordance with a first embodiment of the subject invention.

FIGURE 4 shows an attenuator circuit having adjustable compensation in accordance with a second embodiment of the subject invention.

FIGURE 5 shows an attenuator circuit having adjustable compensation in accordance with a third embodiment of the subject invention.

FIGURE 6 shows, in simplified form, an attenuator circuit having adjustable compensation in accordance with the second embodiment of the subject invention of FIGURE 4 and further including offset adjustment circuitry.

FIGURES 7 and 8 are further simplified illustrations useful in explaining the operation of the embodiment of FIGURE 6.

FIGURE 9 is an illustration of an alternate embodiment of the arrangement of FIGURE 3.

FIGURE 10 is an illustration of an alternate embodiment of the arrangement of FIGURE 4.

Detailed Description of the Drawing

FIGURE 1 shows a prior art attenuator having adjustable compensation for stray part variations, and exhibiting a 10:1 divider ratio with respect to the amplitude of an input signal under test **S101a**. The circuit employs a resistive voltage divider arrangement consisting of resistors **R101**, **R102**, which are coupled in parallel with capacitors **C101**, **C102**, respectively. The attenuated output signal is developed across resistor **R102** and applied to the input of a buffer amplifier **110**. The nominal input capacitance of buffer amplifier **110** is included in **C102**. Typical values for the circuit components of FIGURE 1 are:

R101 = 900 k Ω	**C101** = 1 picofarad (pf)
R102 = 100k Ω	**C102** = 9 picofarads (pf) (variable)

Unfortunately, variations from the nominal capacitance of input amplifier **110**, stray capacitance of circuit board traces, and tolerances of the components themselves, tend to distort the leading edges of an input waveform. These variations in capacitance are represented in FIGURE 1 as a "ghost" capacitance C_{STRAY} (shown in phantom), and as noted above, distort the signal under test. In this regard, waveforms **S101b** and **S101c** (both shown in phantom) are not separate signals, but are merely different examples of a distorted signal developed at the center tap of voltage divider **R101**, **R102**. For simplicity

of explanation, the signal represented by waveforms **101b** and **101c** is shown as having the same amplitude as input signal **101a**. However, one skilled in the art will quickly recognize that in actual practice, the amplitude of the signal developed at the junction of resistors **R101** and **R102** will be substantially one-tenth of the amplitude of input signal **S101a**.

In FIGURE 1, the compensation adjustment may be done by laser-trimming of capacitor **C102**, or by using a variable capacitor, as shown. In either case, compensation is achieved when **R101** x **C101** = **R102** x (**C102** + C_{STRAY}). U.S. Patent 4,507,618 (Nelson) issued 26 March 1985 discusses adjusting the value of capacitor **C101** or **C102** to compensate for the above-mentioned distortion. If the value of capacitor **C102** is too small with respect to the value of capacitor **C101**, then the low frequencies will be attenuated more than the high frequencies. This condition causes the signal developed at the center tap of voltage divider **R101**, **R102** to have sharp edges as shown in waveform **S101b**. If the value of capacitor **C102** is too large with respect to the value of capacitor **C101**, then the high frequencies will be attenuated more than the low frequencies. This condition causes the signal developed at the center tap of voltage divider **R101**, **R102** to have rounded edges as shown in waveform **S101c**. The effect of changing the compensation by adjusting **C102** is shown in output waveform **S101d**. Unfortunately, a variable capacitor is expensive, unreliable, and requires manual operation, and laser-trimming requires an extra manufacturing procedure. As noted above, the use of a varactor diode for capacitor C102 is undesirable because varactor diodes introduce non-linearity.

FIGURE 2 illustrates another prior art attempt at compensating an attenuator. Elements of FIGURE 2 having similar reference numerals to elements of FIGURE 1, serve a similar function, and need not be described in detail. FIGURE 2 shows the addition of a feedback loop including a variable gain amplifier **220** operating under control of a controller represented as a Digital to Analog Converter (DAC) **225**, and a coupling capacitor C_{COMP}. Changing the gain of amplifier **220** changes the value of the effective capacitance, C_{EFF}, loading the attenuator. If the gain of amplifier **220** is made equal to 0, then the value of $C_{EFF} = C_{COMP}$. If the gain of amplifier **220** is made equal to 1, then the value of $C_{EFF} = 0$. If the gain of amplifier **220** is made equal to -1, then the value of $C_{EFF} = 2\ C_{COMP}$. In the arrangement of FIGURE 2, the value of **C202** is 9pf - C_{COMP}.

The prior art circuit of FIGURE 2 exhibits three problems. First, phase delays in the feedback loop of amplifiers **210** and **220** increase with increasing frequency, and become unacceptable at some high frequency. Second, variable gain amplifier **220** adds noise directly to the signal under test. Third, variable gain amplifier **220** provides compensation by acting as a current sink for high frequency components of the signal under test, and in this role it has to absorb a significant amount of high frequency current.

The subject invention will now be described with respect to embodiments shown in FIGURES 3, 4, and 5. In each of these three embodiments, compensation is achieved by adjusting the attenuation of the low frequency components of the signal, rather than by using the prior art method of adjusting the high frequency components.

The circuitry of FIGURE 3 employs low frequency feedback to achieve compensation, thus avoiding the phase delay problem of the prior art. It differs from the circuitry of FIGURE 2 in that **R302** is no longer coupled to ground. Instead, the output of a variable gain amplifier **320** serves as a point of signal return and is DC-coupled to the lower end of **R302**. This arrangement solves the noise problem, referred to above, in that the noise is improved because low frequency feedback is narrow band, typically < 1MHz bandwidth, and so only a small portion of the noise of amplifier **320** is fed into the signal path. It also solves the high frequency current problem because capacitor **C302** returns to ground and because amplifier **320** does not act as a sink for high frequency components of the signal under test.

Waveform **S301a** represents the input signal under test. Waveforms **S301b** and **S301c** represent the range of adjustment available in a signal developed at the input of amplifier **310**. Waveforms **301b'** and **301c'** represent the range of adjustment in the output signal developed at the output terminal of amplifier **310**. Finally, waveform **S301d** shows the compensated signal developed at the output terminal of amplifier **330**.

One skilled in the art will realize that amplifier **310** must have sufficient dynamic range to accommodate the capacitance variations. Moreover, this arrangement requires the use of a gain compensation stage **330**, operating under control of a DAC **335**. It is noted that the addition of gain compensation stage **330** is not burdensome because most modern oscilloscope designs already include such a stage. It is also noted that amplifier 330, and DAC 335 could be eliminated so long as their function is maintained by some other means.

For example, the gain may be adjusted by digital multiplication (i.e., number crunching). A characteristic of the arrangement of FIGURE 3 is that the input resistance changes with compensation adjustment. The input resistance is said to change because a portion of the compensation signal applied to the input terminal of amplifier **310** is also developed at input terminal **301**, thereby affecting current flow into and out of input terminal **301**. This characteristic is not considered to be unduly troublesome when the divider ratio is 10:1, because a 10% compensation range results in only a 1% change in input resistance.

FIGURE 4 is an illustration of circuitry employing a solution for the change of resistance effect. The circuitry of FIGURE 4 takes advantage of a requirement of many attenuators to provide a second attenuation range, e.g., a selectable divide-by-100 stage, by applying an opposite resistance compensation in that stage.

Referring to FIGURE 4, resistor **R405** in series combination with resistor **R406'** forms a 10:1 voltage divider (where **R406'** refers to the combination of **R406** in shunt with the series combination of **R403** and **R404**). A second 10:1 voltage divider, formed by the series combination of resistor **R403** and resistor **R404**, is coupled to the center tap of voltage divider **R405**, **R406'**. This results in a cascade connection of two divide-by-10 arrangements for a total divider ratio of 100:1.

Switch **SW1** selects between a divide-by-10 mode of operation and a divide-by-100 mode of operation. In divide-by-10 mode, the input signal resistive divider path comprises resistors **R401** and **R402**. An output signal is taken from the center-tap of the divider (i.e., the junction of resistors **R401** and **R402**). Low frequency compensation is applied at the bottom of the resistive divider (i.e., the second end of resistor **R402**). As noted above, a portion of the low frequency compensation signal is also felt at input **401**. To compensate for the undesirable effects caused by the application of this signal at input terminal **401**, an equal and opposite cancellation signal is applied to input terminal **401** via a second path comprising resistors **R405** and **R406'**. Amplifier **440** has a gain of -1, and is employed to provide the above-mentioned opposite resistance compensation by applying the cancellation signal to the bottom of the second resistive divider. The two signals substantially cancel at input terminal **401**. Thus, because current flow into and out of input terminal **401** is

substantially unaffected, it follows that the input resistance seen at terminal **401** remains constant, independent of the compensation adjustment (i.e., the gain of amplifier **420**).

When switch **SW1** selects divide-by-100 mode, the input signal resistive divider path comprises resistors **R405**, **R406**, **R403** and **R404**. An output signal is taken from the center-tap of the cascaded divider (i.e., the junction of resistors **R403** and **R404**).

It should be noted that the value loaded into DAC **425** depends upon the position of switch **SW1** for two reasons. First, the 10X and 100X attenuators may have different stray capacitance errors, and thus require different compensations. Second, The inversion provided by amplifier **440** will invert the polarity of the compensation. That is, a gain of amplifier 420 such that $G_{420} > 0$ decreases attenuation of low frequency (LF) signals in the 10X attenuation path, but increases attenuation of the low frequency signals in the 100X path. One skilled in the art will realize that switch **SW1** is preferably an electronic switch controlled by a controller (not shown) that also controls the value loaded into DAC **425**.

As noted above, a portion of the low frequency compensation signal is also felt at input **401**. To compensate for the undesirable effects caused by the application of this signal at input terminal **401**, an equal and opposite cancellation signal is applied to input terminal **401** via the path comprising resistors **R401** and **R402.** As noted above, because amplifier 440 has a gain of -1, the cancellation signal applied to the bottom of the first resistive divider (i.e., the bottom of resistor **R402)** is equal and opposite to the compensation signal. Once again, the two signals substantially cancel at input terminal **401**. Thus, because current flow into and out of input terminal **401** is substantially unaffected, it follows that the input resistance seen at terminal **401** remains constant. In the circuitry of FIGURE 4, input resistance is constant with any DAC setting but only the one attenuator currently in use is compensated.

Values for the elements of FIGURE 4 are:

R401 = 1.8 MΩ	**C401** = 1 picofarad (pf)
R402 = 200 kΩ	**C402** = 9 picofarads (pf)
R403 = 1.8 MΩ	**C403** = 1 picofarad (pf)
R404 = 200 kΩ	**C404** = 9 picofarads (pf)
R405 = 1.8 MΩ	**C405** = 8.1 picofarads (pf)
R406 = 222 kΩ	**C406** = 1 picofarad (pf)

Although the circuitry of FIGURE 5 also employs low frequency compensation, that compensation is applied at a later amplifier stage as a feed forward technique. The output signal **501a'** of a buffer amplifier **510** is applied to a high frequency signal path comprising resistor **R506** and to a low frequency signal path. The low frequency signal path comprises a variable gain amplifier **520** operating under control of a DAC **525**, an R-C low pass filter including resistor **R507** and capacitor **C507**, a buffer amplifier **540**, and a series resistor **R508**. Signals from the high frequency and low frequency signal paths are summed at the junction of resistors **R506** and **R508** and applied to a further variable gain amplifier **530** operating under control of a DAC **535**. In this design, the additional R-C time constant provided by R-C network **R507**, **C507** is matched to the time constant of the input R-C network **R501**, **C501** and **R502**, **C502**. In this example **R507** has a value of 9kΩ and capacitor **C507** has a value of 100 pf.

In operation, the gain of variable gain amplifier **520** determines whether the output signal of amplifier **540** appears more like waveform **S501e**, or more like waveform **S501f**. The output signal from DAC **525** controls variable gain amplifier **520** to properly shape the low frequency signal, such that when summed with the signal in the high frequency path, the resultant combined signal causes output amplifier **530** to produce a compensated waveform **S501d** at its output terminal. The apparatus of FIGURE 5 has the following three advantages. First, it does not modify the input resistance. Second, because it operates on the low frequency components of the signal, variable gain amplifier **520** does not have to sink high frequency current. Third, this design reduces noise in the signal path because the output signal of variable gain amplifier **540** is low pass filtered by R-C network **R507**, **C507**.

FIGURE 6 is an illustration of a compensation arrangement for an attentuator in accordance with the subject invention, wherein the arrangement further includes offset adjustment circuitry. The topology of FIGURE 6 is substantially the same as that of FIGURE 4 with the exceptions that an Adder **650** has been included, and the capacitors are not shown for simplicity and ease of explanation, because an offset signal has only a DC value. All elements of FIGURE 6 that have similar reference numbers to elements of FIGURE 4 serve the same purpose and need not be described again. Referring to FIGURE

6, note that Adder **650** is connected to receive, at a first terminal, the compensation signal from variable gain amplifier **620**. Adder **650** adds a DC V_{OFFSET} signal, received at a second terminal, to the compensation signal and applies the combined signal to resistor **R602** and amplifier **640**. The arrangement of FIGURE 6 takes advantage of the technique shown in FIGURE 4 of stabilizing the input resistance of the attenuator by applying an opposite resistance compensation, and extends the technique to adjust for offset in the input signal.

While the attenuator topology is discussed in terms of 10X and 100X attenuation ratios, one skilled in the art will readily understand that the teachings herein apply equally to other attenuation ratios. The effect of an offset signal on a 10 X attenuator is discussed below with reference to FIGURE 7, and the effect of an offset signal on a 100 X attenuator is discussed with reference to FIGURE 8.

The circuit of FIGURE 7 is redrawn from FIGURE 6 to put emphasis on the 10X attenuation path. In this regard, the selection switch **SW1** and the 100X output path have been removed. Note also that resistors **R603** (1.8 MΩ), **R604** (200kΩ), and **R605** (222kΩ) have been combined into their equivalent resistance **R706EQ** having a value of 200 kΩ

A voltage **v** is calculated in terms of the input voltage V_{IN} and the adjustment voltage V_{OFFSET}. One can treat these voltages as being developed in independent voltage sources. We may use superposition to find the contribution of each source to the composite voltage **v,** with the other source set to zero. It should be noted that even if source V_{IN} has a non-zero source resistance, changes in V_{OFFSET} will not cause any changes in the voltage seen at the input node. That is, the input node is a virtual ground with respect to V_{OFFSET}.

For $V_{OFFSET} = 0$

EQ1: $v = [(V_{IN} - Gv)k + Gv]$

EQ2: $$v = \frac{kV_{IN}}{1-(1-k)G}$$

Where **k** is the inverse of the attenuation ratio (0.1 in this example); and **G** is the gain of variable gain amplifier **720**.

For $V_{IN} = 0$

EQ3: $v = [(V_{OFFSET} + Gv)(1-k)]$

EQ4: $v = \frac{(1-k)V_{OFFSET}}{1-(1-k)G}$

Where **k** is the attenuation ratio (0.1 in this example); and
G is the gain of variable gain amplifier **720**.

Combining both expressions for **v** (i.e., **EQ2** and **EQ4**) yields:

EQ5: $v = \frac{kV_{IN} + (1-k)V_{OFFSET}}{1-(1-k)G}$

but, v = 0 when:

EQ6: $kV_{IN} = -(1-k)V_{OFFSET}$

solving for V_{OFFSET} yields:

EQ7: $V_{OFFSET} = \frac{-kV_{IN}}{1-k}$

Note that the expression of **EQ7** is independent of G, the gain of variable gain amplifier **720**. Thus, for the 10X attenuator (k=0.1):

EQ8: $V_{OFFSET} = \frac{-.1}{.9}V_{IN}$

EQ9: $V_{OFFSET} = -0.1111111V_{IN}$

Thus, a V_{OFFSET} of -10 Volts can be used to correct an offset of 90 volts in a signal applied to input terminal **701** of 10X attenuator **700**.

This is in contrast to typical offset ranges as known from the prior art. These offset ranges are designed into high speed buffer amplifiers and extend between ± 1 volt. In such a system, the maximum voltage that could be offset at the input node to a 10X buffer amplifier using offset in the buffer amplifier would be ±10 volts.

Thus, by use of this aspect of the subject invention with an offset voltage source having a ± 10 volt offset range, a nine-fold improvement in offset adjustment is achieved, while simultaneously relaxing design requirements in the dynamic range of the input buffer amplifier.

The circuit of FIGURE 8 is redrawn from FIGURE 6 to put emphasis on the 100X attenuation path. In this regard, the selection switch **SW1** and the 10X output path have been removed. The analysis is substantially identical to that given above except for the polarity of V_{OFFSET} due to the gain of -1 provided by amplifier **840**, and all steps need not be shown again. Similar equation numbers in the analysis of FIGURE 8, relate to the same point in the analysis given above with respect FIGURE 7.

Where **k** is the attenuation ratio (0.01 in this example); and

G is the gain of variable gain amplifier **820**.

$$\textbf{EQ5':}\quad v = \frac{kV_{IN} - (1-k)V_{OFFSET}}{1-(1-k)G}$$

but, v = 0 when:

$$\textbf{EQ6':}\quad kV_{IN} = (1-k)V_{OFFSET}$$

solving for V_{OFFSET} yields:

$$\textbf{EQ7':}\quad V_{OFFSET} = \frac{kV_{IN}}{1-k}$$

As above, the expression of **EQ7'** is independent of G, the gain of variable gain amplifier **820**. Thus for the 100X attenuator (k=0.01):

$$\textbf{EQ8':}\quad V_{OFFSET} = \frac{.01}{.99}V_{IN}$$

$$\textbf{EQ9':}\quad V_{OFFSET} = 0.0101010101V_{IN}$$

Thus, a V_{OFFSET} of 10 volts can be used to correct an offset of 990 volts in a signal applied to input terminal **801** of 100X attenuator **800**.

FIGURE 9 shows an embodiment of the invention that is similar to that of FIGURE 3, with the exception that capacitor **902** is returned to the output terminal of amplifier **910**. Amplifier **910** exhibits a large negative gain, and the gain range of amplifier **920** is centered around a nominal gain of 1 instead of a nominal gain of 0. The elements of FIGURE 9 bearing similar reference numerals to those of FIGURE 3 serve the same purpose and need not be described again.

It is felt that the large negative gain of amplifier **910** with feedback makes its input appear to be a virtual ground. This virtual ground provides several benefits. First, the input resistance is simply that of resistor **R901**, and is not affected by changing the compensation. Second, no signal voltage appears across, and no signal current flows through, capacitance C_{STRAY}. Thus, compensation is needed only to correct for component value errors in resistors **R901** and **R902**, and capacitors **C901** and **C902**. Third, further attenuation ranges may be switched into place by using switches connected to the virtual ground, thereby allowing the use of switches having relatively high values of C_{STRAY}.

FIGURE 10 is an embodiment of the invention that is similar to that of FIGURE 4, except that switch **SW1** is eliminated and resistor **R1005** is substituted for the divide by 100 attenuator arrangement. In the apparatus of FIGURE 10, resistors **R1005** provides a path for the inverted compensation signal to be applied to input terminal **1001**. Cancellation of the compensation signal and the inverted compensation signal at input terminal **1001** maintains a stable input resistance in the same manner as explained above.

What has been described is a method and apparatus for compensating a high frequency attenuator, wherein the low frequency components of the signal under test are adjusted to accomplish the compensation. An additional embodiment of the invention, including a method and apparatus for adjusting offset has also been described.

While the invention has been described with respect to attenuators used in test and measurement instruments such as oscilloscopes, logic analyzers, communications analyzers, spectrum analyzers, and the like, it is herein recognized that the invention is also applicable to attenuators employed in other fields of use. Use outside the test and measurement field of use, and inside the test and measurement field of use, are both deemed to lie within the scope of the following claims.

The following other modifications are considered to lie within the scope of the claims. For example, means other than a DAC may be used for controlling variable gain amplifier **320, 420, 520, 620, 720, 820, 920**. A gain for amplifier **440, 640, 740, 840, 1040** of other than -1 (with a corresponding change in the ratio of the individual attenuator input resistances) still accomplishes R_{IN} compensation. Circuitry with more than two attenuators is envisioned. A variable gain amplifier with a differential output may preferably be used rather than a variable gain amplifier followed by an amplifier having a gain of -1. An RL filter rather than an RC filter may be employed. A resistive divider from the variable gain amplifier output to ground may be used to reduce sensitivity to fixed errors in the output signal of the variable gain amplifier. Output variable gain amplifier **330** and DAC **335** could be replaced by "number crunching" circuitry.